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EXAMINER	
MISIURA, BRIAN THOMAS	
ART UNIT	**PAPER NUMBER**
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/732,722	EATON, BILL	
	Examiner	Art Unit	
	Brian T. Misiura	2111	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 June 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-48* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-48* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Detailed Action

Response to Arguments

Regarding the claim objection and 112 rejection of Claims 10, 22, and 23, the Examiner acknowledges the amendments to the Claims and the above objection/rejection have been overcome. Therefore the above objection/rejection have been withdrawn.

Regarding the 112 rejection against Claim 36, the Examiner acknowledges the amendment to this claim and the 112 rejection has been overcome. Therefore, the 112 rejection of claim 36 has been withdrawn.

Regarding the 112 rejection against Claims 37-42, the Examiner acknowledges the amendment to these claims and the 112 rejection has been overcome. Therefore, the 112 rejection of Claims 37-42 has been withdrawn.

Applicant's arguments filed 6/28/2007 have been fully considered but they are not persuasive.

Page 14 of 19 of the Applicants Remarks/Arguments contains the following section: "Schutte appears to describe a bus system wherein any of the alleged integrated circuits may control the clock signal, either as a master, or as a slave simultaneous with the master by delaying the rising edge f the clock signal (see Col. 8, Lines 43-47)." The Examiner points out that above cited section of the Schutte reference begins with the word "**Optionally**"; therefore it is simply an alternate embodiment to the invention disclosed in the Schutte reference. The language of the Applicant's independent claims is broad enough that the Schutte reference reads upon the limitations related to the above argument.

Page 15 of 19 of the Applicants Remarks/Arguments contains the following section: "With particular respect to dependent claims 6, 18, 29, 39, and 45, it does not appear that the Schutte reference describes the limitation of communicating a continuous clock signal generated by the multiple integrated circuit controller. The Examiner suggests that the continuous clock signal is the unvarying, steady signal illustrated in Figure 5 of the Schutte reference during high-speed mode."

In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., "However, continuous clock timing, as set forth in the present invention, refers to maintaining the oscillating clock signal beyond periods of data transmission, i.e. continuously, as is illustrated in Figure 3 of the present disclosure. (page 15 second paragraph)" and "the SCLk shows no clock oscillations, and is thus not continuous, as defined in the present disclosure and claimed. (page 15 third paragraph)") are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993). Claim 6 includes the broad claim limitation: "wherein the clock signal link is further configured to communicate a continuous clock signal". The claim does not include the limitations mentioned by the Applicant in the arguments presented above. Therefore the Examiner gave the claim its broadest interpretation as it was broadly claimed. Schutte provides an 'uninterrupted' clock signal as disclosed in figure 5 Hs-mode.

Page 17 of 19 of the Applicants Remarks/Arguments presents a paragraph stating "one skilled in the art would not be motivated to combine the differential signaling features of the Lattice reference with the bus system set forth in the Schutte reference." The Examiner respectfully disagrees with this statement. Both the I2C specification and the Lattice/Wikipedia documents provide evidence of high-speed signaling over their communication links. Further the rejection below provided several motivations for one of ordinary skill in the art to make the combination.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-9, 11, 12, 15-21, 24, 26-34, and 37-48 are rejected under 35 U.S.C. 102(b) as being anticipated by Schutte U.S. Patent No. 6,092,138.

Per Claims 1 and 24, Schutte discloses:

- a multiple integrated circuit controller configured to initiate and control data transactions between the multiple integrated circuit controller and integrated circuits (figure 1 numerals 10a-e represent stations, any of the stations wanting to start communication can become a master station, which would then assume the role as the 'integrated circuit controller' – column 6 lines 11-22);
- a data link configured to communicate the data transactions between the multiple integrated circuit controller and one or more of the integrated circuits (column 3 line 66 – column 4 line 9, figure 1 numeral 12a-b, SDA and SDAH represent data buses), the multiple integrated circuit controller including a first push-pull driver to drive the data transactions (column 14, lines 43-54, figure 6 numerals 66, 67, and SDA);
- and a clock signal link configured to communicate a clock signal generated by only the multiple integrated circuit controller to the integrated circuits (column 3 line 66 – column 4 line 9, figure 1 numeral 12a-b, SCL and SCLH represent clock buses – once a station becomes the master station (the multiple integrated circuit controller), that station controls the data and clock lines), the multiple integrated circuit controller including a second push-pull driver to drive the clock signal (column 14 lines 55-63, figure 6 numerals 63 and 64).

Per Claim 2, Schutte discloses wherein the data link and the clock signal link form a two-wire control data bus (column 1 lines 22-26, figure 1 – the I2C bus is that of a two-wire bus).

Per Claims 3, 15, 26, Schutte discloses wherein the data link is further configured to communicate write data from the multiple integrated circuit controller to one or more of the integrated circuits (column 6 lines 11-16, figure 1 – the master station utilizes the read/write bit to indicate what type of data communication will take place any of the stations can act as a master and when the master can communicate both read and write transactions with any of the other stations).

Per Claims 4, 16, 27, Schutte discloses wherein the data link is further configured to communicate read data from one or more of the integrated circuit to the multiple integrated circuit controller (column 6 lines 11-16, figure 1 – the master station utilizes the read/write bit to indicate what type of data communication will take place).

Per Claims 5, 17, 28, Schutte discloses wherein the multiple integrated circuit controller is further configured to control a write data transaction from the multiple integrated circuit controller to a first integrated circuit via the data link, and control a read data transaction from a second integrated circuit to the multiple integrated circuit controller via the data link (column 6 lines 11-22, figure 1 – any of the stations can act as a master and when the master can communicate both read and write transactions with any of the other stations).

Per Claims 6, 18, 29, 39, and 45, Schutte discloses wherein the clock signal link is further configured to communicate a continuous clock signal generated by the multiple integrated circuit controller to one or more of the integrated circuits (figure 5 – SCLk takes the form of a continuous clock signal during high speed mode (Hs-mode)).

Per Claims 7, 19, 30, 40, and 46, Schutte discloses wherein the clock signal link is further configured to communicate a pulsed clock signal generated by the multiple integrated circuit controller to one or more of the integrated circuits (figure 5 – SCLk takes the form of a pulsed clock signal during the first 9 clock signals).

Per Claims 8, 20, 31, 41, and 47, Schutte discloses wherein the data link is further configured to communicate error check data between the multiple integrated circuit controller and one or more of the integrated circuits (column 6 lines 35-50, figure 1 – the acknowledge bit qualifies as error check data).

Per Claims 9, 21, 32, 33, 42, and 48, Schutte discloses

- wherein the multiple integrated circuit controller is further configured to communicate a unique target identifier via the data link to initiate a data transaction with an integrated circuit that has an address identified by the unique target identifier (column 6 line 11-22, figure 1 – if the address supplied by the master station matches that of a slave station then that slave station responds to the communication accordingly);
- in an event that the data transaction is a write data transaction, the data link is further configured to communicate the data from the multiple integrated circuit controller to the identified integrated circuit; and in an event that the data transaction is a read data transaction, the data link is further configured to communicate the data from the identified integrated circuit to the multiple integrated circuit controller (column 6 lines 11-24, figure 1 - the master station utilizes the read/write bit to indicate what type of data communication will take place; any of the stations can act as a master and when acting as the master can communicate both read and write transactions with any of the other stations).

Per Claim 11, Schutte discloses:

- a clock signal output configured to communicate a clock signal to integrated circuits via a first data link of a data bus (column 12 lines 44-58, figure 5);
- a first push-pull driver configured to drive the clock signal on the first data link (column 14 lines 55-63, figure 6 numerals 63 and 64);
- a data input/output configured to communicate data between the multiple integrated circuit control and one or more of the integrated circuits via a second data link of the data bus (column 6 lines 11-22, figure 1);
- and a second push-pull driver configured to drive the data on the second data link (column 14, lines 43-54, figure 6 numerals 66, 67, and SDA).

Per Claims 12 and 34, Schutte discloses the multiple integrated circuit control as recited in claim 11 implemented as a single-ended interface control circuit (the system of Schutte is believed to be that of a single-ended system based fact well known in the art that the I2C transmission protocol uses single-ended signaling (this argument is further supported by the included document titled "Single-ended signaling"). Additionally, the lack of Schutte distinctly disclosing the system as using a differential signaling method also supports the reasoning for the signaling of Schutte to be that of single-ended).

Per Claims 37 and 38, Schutte discloses all the limitations presented in this claim. Regarding the computer readable media, Schutte discloses a control/function unit **61** that is coupled to both the data and clock bus drivers, therefore overseeing the communications occurring on those buses. The remaining limitations have been previously rejected with respect to Claims 1, 3, and 4. Please refer to Claims 1, 3, and 4 for explanation of rejection.

Per Claims 43 and 44, the limitations of these claims have already been rejected with respect to Claims 1, 3, and 4. Please refer back to the rejection of those claims for explanation.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 10 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Schutte U.S. Patent No. 6,092,138 in view of Kawamoto U.S. Patent No. 6,967,744.

Per Claims 10 and 22, Schutte does not distinctly disclose the I2C controller as being located within a printing device.

- However, it would have been obvious to one having ordinary skill in the art at the time of the applicants claimed invention to incorporate the I2C protocol setup of Schutte into a printing device in order to benefit from the advantages that an I2C bus has over other conventional bus systems. Motivation for the combination can be seen in

Kawamoto, where an I2C controller and system is present within an image processing apparatus (column 3 lines 1-15, column 4 lines 15-31, and figure 1).

Claim 13, 14, 25, and 35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Schutte U.S. Patent No. 6,092,138 in view of Lattice Semiconductor Corporation, "Differential Signaling" – dated May 2001 (hereafter referred to as Lattice).

Per Claims 13 and 35, Schutte does not distinctly disclose the multiple integrated circuit control as recited in claim 11 implemented as a low voltage differential signaling (LVDS) interface control circuit.

- However, it would have been obvious to one having ordinary skill in the art at the time of the applicants claimed invention to implement the system of Schutte as that of a LVDS. This combination is simply the alternative to using single-ended signaling and is a matter of design choice. Lattice provides several scenarios when using differential signaling would be beneficial. A few of the scenarios include: when the signals are small, when there is a lot of noise, when signals need to run over a distance, and when the signal source is balanced to begin with (page 4). Based on the advantages of using differential signaling as outlined by Lattice, it would have been obvious to implement the system of Schutte as that of a LVDS.

Per Claims 14, 25, Schutte does not disclose a multiple integrated circuit control as recited in claim 11 implemented as a low voltage differential signaling interface control circuit, wherein: the first data link is a differential clock signal link configured to communicate the clock signal as a low voltage differential clock signal; and the second data link is a differential data link configured to communicate the data as a low voltage differential data signal.

However, please refer to the rejection of Claims 13 and 35 for explanation as to why it would have been obvious to implement the system of Schutte as a differential signaling system. If the system of Schutte has been implemented as a differential signaling system then both the clock and data signal lines would be differential signal lines as claimed in the present application.

Claim 23 is rejected under 35 U.S.C. 103(a) as being unpatentable over Schutte U.S. Patent No. 6,092,138 in view of Baker et al. U.S. Patent No. 7,168,00.

Per Claim 23, Schutte discloses the multiple integrated circuit control implemented within an electronic apparatus, but does not distinctly disclose the electronic apparatus as being an application-specific integrated circuit (ASIC).

- However, Baker discloses an I2C bus master embedded within an ASIC device (column 3 lines 57-61, column 4 lines 23-37, figures 1 and 2).

It would have been obvious to one having ordinary skill in the art at the time of the applicants claimed invention to combine the multiple integrated circuit control of Schutte into an ASIC device disclosed by Baker in order to create an ASIC device with an embedded I2C bus master. The combination would have been obvious in order to reduce production costs.

Claim 36 is rejected under 35 U.S.C. 103(a) as being unpatentable over Schutte U.S. Patent No. 6,092,138 in view of Oppendahl, U.S. Patent No. 5,500,861.

Per Claim 36, Schutte discloses:

- communicating a data transaction start indication from the multiple integrated circuit control to the integrated circuits (column 5 lines 49-67, column 6 lines 11-28, figure 1 and 2 – start condition);
- communicating a unique target identifier to initiate the data transaction with an integrated circuit that is identified by the unique target identifier (column 6 lines 11-16, figure 1 – address of a "slave" station);
- communicating control data from the multiple integrated circuit control to define the data transaction with the identified integrated circuit (column 6 lines 11-16 – read/write bit);
- communicating the data between the multiple integrated circuit control and the identified integrated circuit, wherein the multiple integrated circuit control is a data sending device and the identified integrated circuit is a data receiving device in an event that the data is communicated from the multiple integrated circuit control to the identified integrated circuit, further wherein the multiple integrated circuit control is the data receiving device and the identified integrated circuit is the data sending device in an event that the data is communicated from the identified integrated circuit to the multiple integrated circuit control (column 6 lines 11-24, figure 1 - the master station utilizes the read/write bit to indicate what type of data communication will take place; any of the stations can act as a master and when acting as the master can communicate both read and write transactions with any of the other stations);
- communicating a data acknowledgement from the data receiving device to the data sending device to indicate receipt of the data and the data parity bit (column 6 lines 35-50, figure 1 – acknowledge bit);
- and communicating a data transaction stop indication from the data sending device to the data receiving device to indicate receipt of the data acknowledgement (column 6 lines 29-35, figures 1-5).

Schutte does not disclose: a control parity bit or a data parity bit.

- However, Oppendahl discloses both control parity bits and data parity bits (column 4 lines 51-56, column 5 lines 9-16).

It would have been obvious to one having ordinary skill in the art at the time of the applicants claimed invention to incorporate the parity bits of Oppendahl into the system of Schutte. The combination would have obvious because it adds an extra level of data integrity to the system which is something that any system designer would welcome assuming that the resources to do so are available.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brian T. Misiura whose telephone number is (571) 272-0889. The examiner can normally be reached on M-F 8:00-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Rinehart can be reached on (571) 272-3632. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Paul R. Myers

PAUL R. MYERS
PRIMARY EXAMINER

BTM
9/14/2007